AMENDMENTS TO THE CLAIMS

Claims 1-13 (Cancelled).

14. (Currently Amended) A method of forming a semiconductor device, the method comprising the steps of:

forming a layer of insulation material over a semiconductor substrate, the layer of insulation material having a top surface, the semiconductor substrate having a top surface;

etching the layer of insulation material to form a plurality of trenches in the layer of insulation material, each trench having a depth measured normal to the top surface of the substrate, a width, and a length that is many times greater than the width, directions associated with the depth, width, and length being orthogonal to each other, the top surface of the layer of insulation material having a trench region that lies between adjacent trenches in the layer of insulation material, each trench having a bottom surface vertically spaced a first distance apart from the top surface; and

etching the layer of insulation material and the plurality of trenches to lower the top surface of the layer of insulation material in the trench region to form a trench surface that lies below and parallel to the top surface of the layer of insulation material, and to lower the bottom surface of each trench to form a lowered bottom surface that is vertically spaced a second distance apart from the top surface of the layer of insulation material, the second distance being greater than the first distance.

15. (Previously Presented) The method of claim 14 wherein the step of etching the layer of insulation material and the plurality of trenches includes the steps of:

forming a layer of masking material on the layer of insulation material;

patterning the layer of masking material to expose a portion of the top surface of the layer of insulation material and the plurality of trenches; and

anisotropically etching the layer of insulation material and the plurality of trenches.

16. (Previously Presented) The method of claim 14 and further comprising the steps of:

forming a layer of conductive material on the layer of insulation material, the layer of conductive material filling up the trenches; and

planarizing the layer of conductive material to form a conductive region, the conductive region having a top surface that is substantially planar with the top surface of the layer of insulation material, the conductive region in the trenches forming a plurality of bottom fingers with bottom surfaces that lie parallel to the top surface of the layer of insulation material.

17. (Previously Presented) The method of claim 16 wherein the conductive region is formed to have a number of loops that lie substantially in a same plane, the loops being electrically connected together.

18. (Previously Presented) The method of claim 16 wherein a top surface of a single contact is directly connected to the bottom surfaces of the plurality of bottom fingers.

19. (Previously Presented) The method of claim 16 wherein a top surface of a single via is directly connected to the bottom surfaces of the plurality of bottom fingers.

20. (Previously Presented) The method of claim 16 wherein the layer of conductive material includes:

a layer of barrier material formed on the layer of insulation material;

a layer of seed material formed on the layer of barrier material; and

a layer of copper formed on the layer of seed material.

Claims 21-32 (Cancelled).

33. (Previously Presented) The method of claim 14 wherein the lowered bottom surface exposes a nonconductive material.

34. (Previously Presented) The method of claim 33 wherein the lowered bottom surface exposes a conductive material, an exposed area of the nonconductive material being substantially greater than an exposed area of the conductive material.

35. (Previously Presented) The method of claim 34 wherein the conductive material is a top surface of a via.

36. (Previously Presented) The method of claim 34 wherein the conductive material is a top surface of a contact.

37. (Previously Presented) The method of claim 34 and further comprising the steps of:

forming a conductive layer on the layer of insulation material, the conductive layer filling up the trenches; and

planarizing the conductive layer to form a conductive region, the conductive region having a top surface that is substantially planar with the top surface of the

layer of insulation material, the conductive region in the trenches forming a plurality of bottom fingers with bottom surfaces that lie parallel to the top surface of the layer of insulation material.

38. (Cancelled)

39. (Previously Presented) A method of forming a semiconductor device, the method comprising the steps of:

forming a layer of insulation material over a semiconductor substrate, the layer of insulation material having a top surface;

etching the layer of insulation material to form a plurality of trenches in the layer of insulation material, the top surface of the layer of insulation material having a trench region that lies between adjacent trenches, each trench having a bottom surface vertically spaced a first distance apart from the top surface; and

etching the layer of insulation material and the plurality of trenches to lower the top surface of the layer of insulation material in the trench region to form a trench surface that lies below and parallel to the top surface, and to lower the bottom surface of each trench to form a lowered bottom surface that is vertically spaced a second distance apart from the top surface, the second distance being greater than the first distance, the lowered bottom surface exposing a nonconductive material and a conductive material, an exposed area of the nonconductive material being substantially greater than an exposed area of the conductive material.

40. (Previously Presented) The method of claim 39 wherein the plurality of trenches lies substantially parallel to each other.

41. (Previously Presented) The method of claim 39 wherein the conductive material is a top surface of a via.

42. (Previously Presented) The method of claim 39 wherein the conductive material is a top surface of a contact.

43. (New) A method of forming a semiconductor device, the method comprising the steps of:

forming a layer of insulation material over a semiconductor structure, the layer of insulation material having a top surface, the semiconductor structure having a top surface;

etching the layer of insulation material to form a plurality of trenches in the layer of insulation material, each trench having a bottom surface; and

etching the layer of insulation material and the plurality of trenches to lower a portion of the top surface of the layer of insulation material to form a trench surface that lies below and parallel to the top surface of the layer of insulation material, and to lower the bottom surface of each trench to form a lowered bottom surface, a portion of the lowered bottom surface of each trench exposing a same conductive structure.

44. (New) The method of claim 43 wherein the plurality of trenches lies substantially parallel to each other.

45. (New) The method of claim 43 and further comprising the steps of:

forming a conductive layer on the layer of insulation material, the conductive layer filling up the trenches; and

planarizing the conductive layer to form a conductive region, the conductive region having a top surface that is substantially planar with the top surface of the

layer of insulation material, the conductive region in the trenches forming a plurality of bottom fingers with bottom surfaces that lie parallel to the top surface of the layer of insulation material.

46. (New) The method of claim 45 wherein the conductive region is formed to have a number of loops that lie substantially in a same plane, the loops being electrically connected together.